WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

an inner circuit driven by a single power voltage; and

a first protective circuit which protects the inner circuit from a surge,

wherein the inner circuit includes: a high voltage-proof circuit section constituted of a first MOS transistor; a low voltage-proof circuit section constituted of a second MOS transistor including a gate insulating film thinner than that of the first MOS transistor; and a second protective circuit directly connected to the low voltage-proof circuit section to protect the second MOS transistor from the surge.

2. The semiconductor integrated circuit according to claim 1, wherein the low voltage-proof circuit section is driven by an inner power voltage obtained by stepping down the single power voltage.

3. The semiconductor integrated circuit according to claim 2, wherein the second MOS transistor is a device which directly receives the inner power voltage.

4. The semiconductor integrated circuit according to claim 2, wherein the second MOS transistor is a device which directly receives data from the high voltage-proof circuit section.

5. The semiconductor integrated circuit according to claim 1, wherein the low voltage-proof circuit

section exchanges data with respect to the high voltage-proof circuit section.

6. The semiconductor integrated circuit according to claim 1, wherein the second protective circuit is constituted of a diode or a diode-connected MOS transistor, and a clamp voltage by the diode or the diode-connected MOS transistor is larger than a maximum value of a voltage range at the time of a usual operation in the low voltage-proof circuit section.

7. A semiconductor integrated circuit comprising:

a high voltage-proof circuit section constituted of a first MOS transistor and driven by a single power voltage; and

a first protective circuit which protects the high voltage-proof circuit section from a surge,

wherein the high voltage-proof circuit section includes: a low voltage-proof circuit section constituted of a second MOS transistor including a gate insulating film thinner than that of the first MOS transistor; and a second protective circuit directly connected to the low voltage-proof circuit section to protect the second MOS transistor from the surge.

8. The semiconductor integrated circuit according to claim 7, wherein the low voltage-proof circuit section is driven by an inner power voltage obtained by stepping down the single power voltage.

9. The semiconductor integrated circuit according

to claim 8, wherein the second MOS transistor is a device which directly receives the inner power voltage.

10. The semiconductor integrated circuit according to claim 8, wherein the second MOS transistor is a device which directly receives data from the high voltage-proof circuit section.

11. The semiconductor integrated circuit according to claim 7, wherein the low voltage-proof circuit section exchanges data with respect to the high voltage-proof circuit section.

12. The semiconductor integrated circuit according to claim 7, wherein the second protective circuit is constituted of a diode or a diode-connected MOS transistor, and a clamp voltage by the diode or the diode-connected MOS transistor is larger than a maximum value of a voltage range at the time of a usual operation in the low voltage-proof circuit section.

13. A semiconductor integrated circuit comprising:

a first inner circuit constituted of a first MOS transistor and driven by a first power voltage;

a second inner circuit constituted of a second MOS transistor including a gate insulating film thinner than that of the first MOS transistor and driven by a second power voltage lower than the first power voltage to exchange data with respect to the first inner circuit;

a first protective circuit directly connected to

the first inner circuit to protect the first MOS transistor from a surge; and

a second protective circuit directly connected to the second inner circuit to protect the second MOS transistor from the surge.

14. The semiconductor integrated circuit according to claim 13, wherein the second MOS transistor is a device which directly receives the second power voltage.

15. The semiconductor integrated circuit according to claim 13, wherein the second MOS transistor is a device which directly participates in the exchange of the data.

16. The semiconductor integrated circuit according to claim 13, wherein the second protective circuit is directly connected to the second MOS transistor.

17. The semiconductor integrated circuit according to claim 13, wherein the second protective circuit is constituted of a resistance and a capacitor, and has a specific time constant, and the time constant is smaller than a transition time of a signal.

18. The semiconductor integrated circuit according to claim 13, wherein the second protective circuit is constituted of a diode or a diode-connected MOS transistor, and a clamp voltage by the diode or the diode-connected MOS transistor is larger than a maximum value of a voltage range at the time of a usual

operation in the second inner circuit.

19. The semiconductor integrated circuit according to claim 13, wherein the second protective circuit is constituted of an analog switch.

20. The semiconductor integrated circuit according to claim 13, wherein the first protective circuit is directly connected to an external terminal, and the second protective circuit is not directly connected to the external terminal.